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EXAMINER	
KALAM, ABUL	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,318	HABA, BELGACEM	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-13,16-26,28-33,35,38-45,47-54 and 56-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-13,16-26,28-33,35,38-45,47-54 and 56-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. In the amendment filed on November 14, 2006, Applicant cancelled claims 10, 14, 15, 27, 34, 36, 37, 46 and 55, and amended claims 1, 8, 25, 32, 47 and 53. Thereby, claims 1-9, 11-13, 16-33, 35, 38-45, 47-54 and 56-59 are pending in the application.

Claim Objections

2. Claim 35 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitation "wherein the outer ends lie outwardly of the attachment portion of the dielectric layer," is claimed in lines 4-5 of the base claim 25.

Claims 1-9, 11-13, 16-26, 28-33, 35, 38-45, are objected to because of the following informalities:

In line 5 of claim 1, please insert a comma (-- , --) between the words "direction" and "an."

In line 6 of claim 1, the phrase "an attachment portion" appears to be a typographical error. Please delete the phrase or make the appropriate corrections to clarify the claimed limitation.

In lines 11-12 of claim 1, the phrase "the second side of the attachment portion" lacks antecedent basis, and thus should be amended to recite -- the attachment portion

--. Note that in line 5 of claim 1, a second side of the dielectric layer, not the attachment portion, has been claimed.

In line 2 of claim 2, the phrase "generally planar" should be amended to recite -- substantially planar --.

In lines 2-3 of claim 4, the limitations "a first direction" and "a second direction" is unclear because of antecedent basis issues. Applicant has already a claimed a first and second direction in lines 4-6 of claim 1. The Office will interpret the limitations as "one direction" and "another direction," respectively.

In line 3 of claim 8, please insert the word -- wherein -- between before the phrase "the offset portion."

In lines 3-5 of claim 8, the limitation of the offset portion extending "generally in the second direction alongside the semiconductor chip", is unclear because from the specification it appears that the offset portion extends in a horizontal direction away from the chip.

In line 2 of claim 13, the phrase "generally horizontally" should be amended to recite -- substantially horizontally --.

In line 4 of claim 25, please insert the word -- and -- between "side" and "outer."

In lines 7-8 of claim 25, the phrase "the second side of the attachment portion" lacks antecedent basis, and thus should be amended to recite -- the attachment portion --. Note that in line 4 of claim 25, a second side of the dielectric layer, not the attachment portion, has been claimed.

In lines 4-5 of claim 32, the phrase "in a second direction" should be amended to recite -- in a first direction --, because there was no previous claim of a first direction in the base claim 25.

In lines 5-6 of claim 32, the phrase "the dielectric element" lacks antecedent basis and should be amended to recite -- the dielectric layer --.

In line 6 of claim 32, the phrase "alongside the semiconductor chip," is unclear because from the specification it appears that the outer ends extend away from the chip rather than alongside the chip, as claimed.

Claims 2-9, 11-13 and 16-24 depend from claim 1 and thus are also objected to.

Claims 26-33, 35 and 38-45 depend from claim 25 and thus are also objected to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-5, 8, 9, 11-13, 16-26, 28-30, 32, 33, 35, 38-45, 47-54 and 57-59** are rejected under 35 U.S.C. 102(b) as being anticipated by **Suminoe et al. (US 6,380,620, cited in previous Office Action, hereinafter, Suminoe)**.

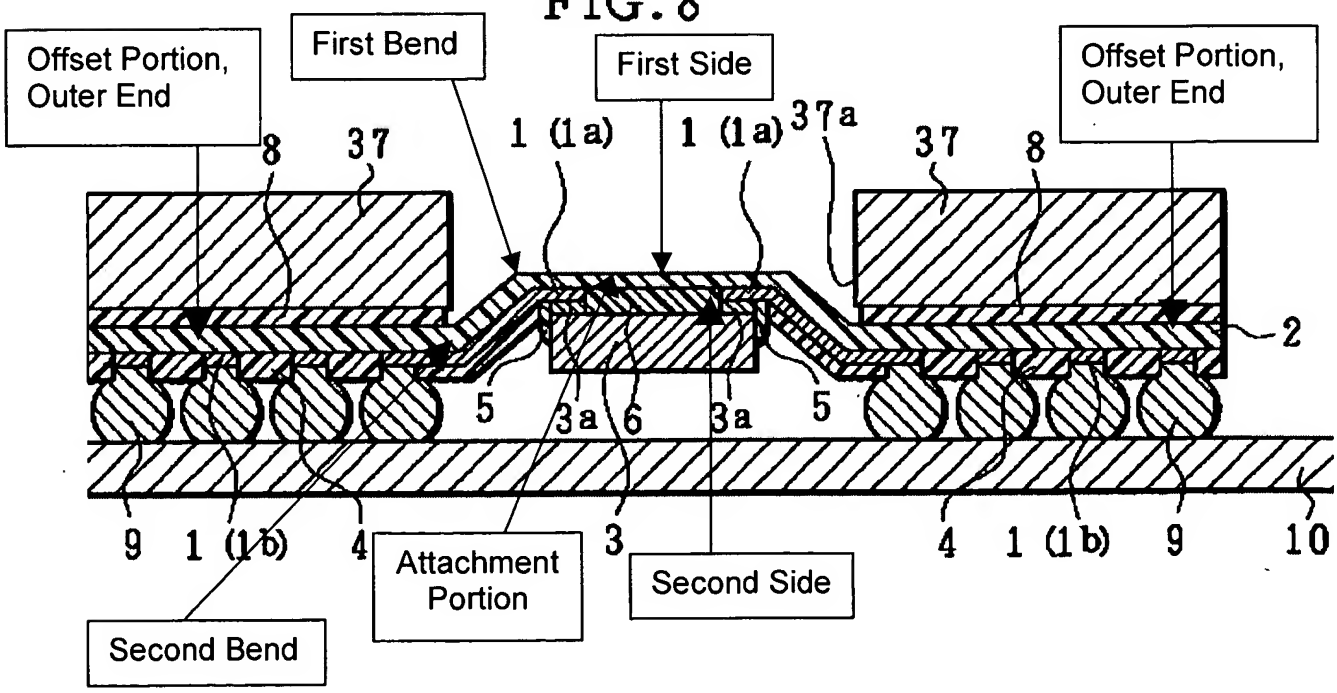
With respect to **claim 1, Suminoe** teaches a microelectronic assembly **(FIG. 8, illustrated below)**, comprising:

a) a dielectric layer **(2)** having an attachment portion **(labeled in FIG. 8 below)**, the dielectric layer **(2)** having a first side **(labeled in FIG. 8 below)** facing a first direction, an oppositely facing second side **(labeled in FIG. 8 below)** facing a second direction, and at least one offset portion **(labeled in FIG. 8 below)** offset from the attachment portion such that the offset portion is skewed in said second direction as compared to said attachment portion;

b) a semiconductor chip **(3)** assembled to the attachment portion, wherein the first side of the dielectric layer **(2)** defines a boundary of the assembly such that the first side is unobstructed **(as shown in FIG. 8 below, the first side of the dielectric layer is exposed)**; and

c) terminal structures **(9)** carried by the offset portion of the dielectric layer **(2)** for connecting the semiconductor chip **(3)** with external circuitry **(10)** lying at a lower level than the attachment portion **(col. 8: lns. 39-65; col. 14: lns. 1-30)**.

FIG. 8



With respect to **claim 2, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** is substantially planar.

With respect to **claim 3, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one bend **(col. 14: lns. 12-14)** between the attachment portion **(labeled in FIG. 8 above)** and the offset portion **(labeled in FIG. 8 above)**.

With respect to **claim 4, Suminoe** teaches the assembly of claim 3 as set forth above, wherein the at least one bend comprises a first bend in one direction and a second bend **(labeled in FIG. 8 above)** in another direction opposite to the one direction.

With respect to **claim 5, Suminoe** teaches the assembly of claims 4 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)** extending in the bend **(FIG. 8)**.

With respect to **claim 8, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the offset portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extends in a horizontal direction.

With respect to **claims 9, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)**, arranged so as to shield the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 11, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the offset portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** comprises a portion that lies outwardly of the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer.

With respect to **claim 12, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one outer end and the terminal structures **(9)** are disposed at the at least one outer end **(FIG. 8)**.

With respect to **claim 13, Suminoe** teaches the assembly of claim 12 as set forth above, wherein the at least one outer end extends substantially horizontally **(FIG. 8)**.

With respect to **claim 16, Suminoe** teaches the assembly of claim 1 as set forth above, further comprising a circuit element **(10)** connected to the terminal structures **(9)** so that the circuit element is disposed underneath the dielectric layer **(2) (FIG. 8)**.

With respect to **claim 17, Suminoe** teaches the assembly of claim 16 as set forth above, wherein the terminal structures **(9)** interconnect the semiconductor chip **(3)** with the circuit element **(10) (FIG. 8)**.

With respect to **claim 18, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** includes traces **(1a, 1b)** connected to the terminal structures **(9)** and connected to contacts **(3a)** of the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 19, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the semiconductor chip **(3)** has a first face with contacts **(3a)** exposed at the first face **(FIG. 8)**.

With respect to **claim 20, Suminoe** teaches the assembly of claim 19 as set forth above, wherein the semiconductor chip **(3)** is assembled to the attachment portion so that the first face faces in an upward direction **(chip 3 is face bonded to the attachment portion, FIG. 8 above)**.

With respect to **claim 21, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** comprises a continuous sheet **(FIG. 8)**.

With respect to **claim 22, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** comprise bonding material **("solder balls," col. 8, lns. 39-42).**

With respect to **claim 23, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** are connected to conductors **(1a, 1b)** extending through the attachment portion **(labeled in FIG. 8 above)**.

With respect to **claim 24, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** comprise solder balls **(col. 5, lns. 49-50).**

With respect to claim 25, Suminoe teaches a microelectronic assembly, comprising:

a) a dielectric layer **(2)** having an attachment portion **(labeled in FIG. 8 above)**, the dielectric layer having a first side, a second side, and outer ends **(all labeled in FIG.**

8 above) lying outwardly of the attachment portion, the outer ends being offset from the attachment portion;

b) a semiconductor chip **(3)** assembled to the attachment portion; and

c) terminal structures **(9)** carried by the outer ends of the dielectric layer **(2)** for connecting the semiconductor chip **(3)** with external circuitry **(10) (FIG. 8, as illustrated above; col. 8: lns. 39-65; col. 14: lns. 1-30)**.

With respect to **claim 26, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** is substantially planar.

With respect to **claim 28, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** has at least one bend **(col. 14: lns. 12-14)** between the attachment portion **(labeled in FIG. 8 above)** and the outer ends **(labeled in FIG. 8 above)**.

With respect to **claim 29, Suminoe** teaches the assembly of claim 28 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend **(both labeled in FIG. 8 above)** in second direction opposite to the first direction.

With respect to **claim 30, Suminoe** teaches the assembly of claims 28 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)** extending in the bend **(FIG. 8)**.

With respect to **claim 32, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the outer ends **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extend substantially in a first direction away from the first side of the dielectric layer **(2)**.

With respect to **claim 33, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the outer ends **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extend substantially horizontally.

With respect to **claim 35, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the outer ends **(labeled in FIG. 8 above)** lie outwardly of the attachment portion of the dielectric layer **(2)**.

With respect to **claim 38, Suminoe** teaches the assembly of claim 25 as set forth above, further comprising a circuit element **(10)** connected to the terminal structures **(9)** so that the circuit element is disposed underneath the dielectric layer **(2) (FIG. 8)**.

With respect to **claim 39, Suminoe** teaches the assembly of claim 38 as set forth above, wherein the terminal structures **(9)** interconnect the semiconductor chip **(3)** with the circuit element **(10) (FIG. 8)**.

With respect to **claim 40, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** includes traces **(1a, 1b)** connected to the terminal structures **(9)** and connected to contacts **(3a)** of the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 41, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the semiconductor chip **(3)** has a first face with contacts **(3a)** exposed at the first face **(FIG. 8)**.

With respect to **claim 42, Suminoe** teaches the assembly of claim 41 as set forth above, wherein the semiconductor chip **(3)** is assembled to the attachment portion so that the first face faces in an upward direction **(chip 3 is face bonded to the attachment portion, FIG. 8 above)**.

With respect to **claim 43, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** comprises a continuous sheet **(FIG. 8)**.

With respect to **claim 44, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the terminal structures **(9)** comprise bonding material **("solder balls," col. 8, lns. 39-42).**

With respect to **claim 45, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the terminal structures **(9)** are connected to conductors **(1a, 1b)** extending through the attachment portion **(labeled in FIG. 8 above)**.

With respect to **claim 47, Suminoe** teaches a microelectronic component, comprising:

a) a dielectric layer **(2)** comprising a continuous sheet having a first side, a second side and an attachment portion **(all labeled in FIG. 8 above)** for assembly with a microelectronic element **(3)**, the microelectronic element being attached to the second side of the continuous sheet and the first side of the continuous sheet being clear of other elements, an offset portion **(labeled in FIG. 8 above)** offset from the attachment portion;

b) terminal structures **(9)** on the dielectric layer **(2)**; and

c) conductors **(1a, 1b)** attached to the terminal structures **(9) (FIG. 8, as illustrated above; col. 8: lns. 39-65; col. 14: lns. 1-30)**.

With respect to **claim 48, Suminoe** teaches the component of claim 47 as set forth above, wherein the terminal structures **(9)** include bonding material **("solder balls," col. 8, lns. 39-42)**.

With respect to **claim 49, Suminoe** teaches the component of claim 47 as set forth above, wherein the dielectric layer **(2)** has at least one bend **(col. 14: lns. 12-14)** between the attachment portion **(labeled in FIG. 8 above)** and the offset portion **(labeled in FIG. 8 above)**.

With respect to **claim 50, Suminoe** teaches the component of claim 49 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend **(both bends labeled in FIG. 8 above)** in second direction opposite to the first direction.

With respect to **claim 51, Suminoe** teaches the component of claim 47 as set forth above, wherein the conductors **(1a, 1b)** comprise a plurality of traces **(FIG. 8)**.

With respect to **claim 52, Suminoe** teaches the component of claim 51 as set forth above, wherein at least one of the traces **(1a, 1b)** is disposed in the bend **(FIG. 8)**.

With respect to **claim 53, Suminoe** teaches the component of claim 49 as set forth above, wherein the attachment portion is substantially horizontal and the offset portion extends downwardly **(illustrated in FIG. 8 above)**.

With respect to **claim 54, Suminoe** teaches the component of claim 47 as set forth above, wherein the offset portion lies outwardly of the attachment portion **(FIG. 8)**.

With respect to **claim 57, Suminoe** teaches the component of claim 47 as set forth above, wherein the terminal structures **(9)** include vias **(52; FIG. 17)** defined by the dielectric layer.

With respect to **claim 58, Suminoe** teaches the component of claim 47 as set forth above, wherein the terminal structures **(9)** include bonding materials **("solder balls," col. 8, lns. 39-42)**.

With respect to **claim 59, Suminoe** teaches the component of claim 47 as set forth above, wherein the terminal structures **(9)** comprise solder balls **(col. 8, lns. 39-42)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 6, 7, 31 and 56** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Suminoe (presented above)**.

With respect to **claims 6 and 31, Suminoe** teaches the microelectronic assembly of claims 1 and 25, respectively, as set forth above, wherein the at least one conductor **(1a, 1b)** extends along the bend of the dielectric layer **(2) (FIG. 8 above)**.

Thus, **Suminoe** teaches all the limitations of claims 6 and 31, with the exception of disclosing: wherein the conductor is arranged to support the bend in the dielectric layer. However, the functional limitation "to support the bend in the dielectric layer," is

implicit because **Suminoe's** device has the same structure as applicant's claimed invention.

Furthermore, an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a deivce is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

With respect to **claims 7 and 56, Suminoe** teaches the microelectronic assembly and component of claims 1 and 47, respectively, as set forth above, wherein the dielectric layer **(2)** comprises a polymeric material **(col. 8: lns. 56-65)** that includes an offset portion **(labeled in FIG. 8 above)**.

Thus, **Suminoe** teaches all the limitations of claim 7 and 56, with the exception of disclosing: forming the offset portion by molding the polymeric material. However, the limitation of forming the offset portion by molding the polymeric material, is a product by process limitation and therefore is given no patentable.

Initially, and with respect to claims 7 and 56, note that a "product by process" claim is directed to the product per se, no matter how actually made. *In re Thorpe et al.,*

227 USPQ 964, (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and no the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Note that Applicant has burden of proof in such cases as the above case law makes it clear.

Response to Arguments

Applicant's arguments with respect to claims 1-9, 11-13, 16-26, 28-33, 35, 38-45, 47-54 and 56-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abul Kalam
Examiner
Art Unit 2814

Nathan W. Ha, PE